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## CLAIMS:

1. Integrated circuit, comprising:
  - at least one processing unit (PU);
  - a cache memory (L2\_bank) having a plurality of memory modules for caching data;
- 5 - remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules.
2. Integrated circuit according to claim 1, wherein said cache memory (L2\_BANK) is a set-associative cache.
- 10 3. Integrated circuit according to claim 1 or 2, wherein said remapping means is adapted to perform the remapping on the basis of a programmable permutation function.
4. Integrated circuit according to claims 1 or 2, wherein said remapping means is adapted to perform the remapping on the basis of a reduction mapping.
- 15 5. Integrated circuit according to claim 1, further comprising:
  - a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2\_BANK), and
- 20 wherein said remapping means is arranged in series with said Tag RAM unit (TagRAM).
6. Integrated circuit according to claim 1, further comprising:
  - a Tag RAM unit (TagRAM) associated to said cache for identifying which data is cached in said cache memory (L2\_BANK), and
- 25 wherein said remapping means is arranged in parallel to said Tag RAM unit (TagRAM).
7. Integrated circuit according to claim 5 or 6, further comprising:

a look up table for marking faulty memory modules.

8. Method of cache remapping in an integrated circuit having at least one processing unit (PU); a main memory (MM) for storing data and a cache memory (L2\_BANK) having a plurality of memory modules for caching data, comprising the step of:
- 5 performing an unrestricted remapping within said plurality of memory modules.